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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,898	04/02/2001	Eric B. Kushnick	CRED 2164	2197

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EXAMINER	
CHEN, TSE W	
ART UNIT	**PAPER NUMBER**
2116	2

DATE MAILED: 03/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,898	KUSHNICK, ERIC B.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The spacing of the lines of the specification is such as to make reading and entry of amendments difficult. New application papers with lines double spaced on good quality paper are required.

2. Claims 1, 7-9, 11-12, 14-17, 19-20, and 26-38 are objected to because of the following informalities: using a comma instead of the conventional semicolon to separate clauses of a claim (e.g., second means clause of claim 1 should end with "... substantially wider than Tp/N**;** and"; and missing the conjunction "and" in claims with more than one clause (e.g., claim 7 should end with "... first pulse sequence***; and*** wherein each first gate...". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-8, 11, 15-16, 20-27, 30, and 34-35 are rejected under 35 U.S.C. 102(a) as being anticipated by Heyne, U.S. Patent 6194928.

5. As per claim 1, Heyne taught an integrated pulse delay generating circuit [FIG. 1] comprising of:

- first means to generate each second pulse in response to a separate first pulse with a first delay adjustable by a first control data and a resolution of Tp/N over a first

range substantially wider than Tp/M, wherein M and N are differing integers greater than one [column 1, lines 38-39; column 3, lines 58-60; column 2, lines 48-50; FIG. 3];

- second means to generate each third pulse in response to a separate second pulse with a delay adjustable by a second control data and a resolution of Tp/M over a second range substantially wider than Tp/N [column 2, lines 6-8; column 3, lines 55-56, lines 61-63; column 1, lines 39-40]; and
- means for generating the first and second control data in response to each pulse of the first pulse sequence [column 1, lines 41-46].[1]

6. As per claims 2 and 5, Heyne taught M and N to be relatively prime [FIG. 3].

7. As per claims 3 and 4, Heyne taught at least one of the first and second ranges to be wider than Tp[2].

8. As per claim 6, Heyne taught the generated third pulse sequence to be periodic [column 2, lines 4-5].

9. As per claim 7, Heyne taught a plurality of first gates connected in series for generating second pulses in response to first pulses wherein each first gate has a switching delay of Tp/N [FIG. 1, item I1; column 3, line 50].

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[1] The control unit comprises of a phase detector and counter for receiving each first pulse and producing the appropriate control data for the two respective delay units [FIG. 2].

[2] The second delay unit comprises of coarse delay elements that are used initially to increment the delay time to the range of the desired delay period. When the desired delay period is exceeded, a coarse delay element is removed and subsequent adjustments are performed with the first delay unit with finer delay elements. Ergo, an ordinary artisan would have inferred that the second delay unit must be designed with a range wider than the expected Tp in order for the initial adjustment to be performed correctly [abstract].

10. As per claim 8, Heyne taught a plurality of second gates connected in series for generating third pulses in response to second pulses wherein each second gate has a switching delay of Tp/M [FIG. 2, item I2; column 3, lines 51-52].

11. As per claims 11 and 16, Heyne taught:

- a plurality of first gates connected in series for generating second pulses in response to first pulses wherein each first gate has a switching delay of Tp/N [FIG. 1, item I1; column 3, line 50]; and
- a plurality of second gates connected in series for generating third pulses in response to second pulses wherein each second gate has a switching delay of Tp/M [FIG. 2, item I2; column 3, lines 51-52].

12. As per claim 15, Heyne taught an integrated pulse delay generating circuit [FIG. 1] comprising of:

- first means to generate each second pulse in response to a separate first pulse with a first delay adjustable by a first control data and a resolution of Tp/N [column 1, lines 38-39; column 3, lines 58-60; column 2, lines 48-50; FIG. 3];
- second means to generate each third pulse in response to a separate second pulse with a delay adjustable by a second control data and a resolution of Tp/M [column 2, lines 6-8; column 3, lines 55-56, lines 61-63; column 1, lines 39-40];
- means for generating the first and second control data in response to each pulse of the first pulse sequence [column 1, lines 41-46][3]; and
- wherein M and N are relatively prime integers greater than one [FIG. 3].

13. As per claims 20-27, 30, and 34-35, Heyne taught apparatus; therefore, Heyne taught method of apparatus.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 9-10, 12-14, 17-19, 28-29, 31-33, and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heyne as applied to claims 8 and 11 above, and further in view of Liedberg, U.S. Patent 5471165.

16. Heyne taught an integrated pulse delay device comprising of two delay units wherein the units comprises of gates connected in series for generating a range of delay periods that can be monitored to produce the appropriate control signals for phase-locking the first input and final output pulses [FIG. 2].

17. However, Heyne did not expressly disclose an extra series of gates for the delay units or a way to monitor and phase-lock the first input pulse sequence with the output pulse sequence from the first gates.

18. Liedberg taught a modular signal processing circuit with means to delay a periodic input signal by utilizing a multitude of delay gates and means to monitor and phase-lock the input and output pulses [FIG. 2; column 4, lines 5-35].

19. As per claims 9, 12, and 17, Liedberg taught the modular pulse delay unit comprising of:

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[3] The control unit comprises of a phase detector and counter for receiving each first pulse and producing the

- M third gates [FIG. 2, item D2] connected in series with second gates [FIG. 2, item D1] for generating a fourth pulse sequence in delayed response to the first pulse sequence [column 3, lines 57-58; column 4, lines 29-35]; and
- wherein each second and third gate has a similar switching delay of Tp/M set by the magnitude of a second control signal applied to all the second and third gates [column 4, lines 24-35; column 5, lines 31-40].

20. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to increase the resolution and accuracy of a pulse delay generating device [see Liedberg: column 1, lines 24-28; column 2, lines 48-54, lines 63-64].

21. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Heyne and Liedberg to provide a pulse delay generating device with a multitude of delay gates connected in series within a phase monitoring and locking system to increase the resolution and accuracy of the generated pulses.

22. As per claims 10, 13, and 18, Heyne taught the monitoring of a phase relationship between the first pulse sequence and the fourth pulse sequence and adjusting the magnitude of the first control signal so that the fourth pulse sequence is phase-locked with the first pulse sequence [FIG. 2].

23. As per claims 14 and 19, Liedberg taught the modular pulse delay unit comprising of:

- plurality of first N gates [FIG. 2, item D1] connected in series for generating a pulse sequence in delayed response to the first pulse sequence [column 3, lines 57-58; column 4, lines 29-35];

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appropriate control data for the two respective delay units [FIG. 2].

- wherein each gate has a switching delay set by the magnitude of a first control signal [column 4, lines 24-35; column 5, lines 31-40]; and
- wherein the first pulse sequence and the generated pulse sequence are monitored and the first control signal is adjusted to phase lock the pulse sequences [column 4, lines 5-35].

24. As per claims 28-29, 31-33, and 36-38, Heyne and Liedberg taught apparatus; therefore, Heyne and Liedberg taught method of apparatus.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Desai, U.S. Patent 6265924, disclosed a system of different delay stages to increase the operating frequency.

b. Kim, U.S. Patent 6388485, disclosed a series of master/slave delay circuits.

c. Saitoh et al., U.S. Patent 5604775, disclosed a phase locked loop circuit utilizing a series of delay units.

d. Arai, U.S. Patent 6259330, disclosed a ring oscillator with a series of delay units.

e. Lu, U.S. Patent 6100735, disclosed a series of delay locked loop circuits.

f. Moloney et al., U.S. Patent 5670904, disclosed a digital delay unit comprising of various blocks of delay elements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (703) 305-8580. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
March 5, 2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
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